THAT WHICH IS CLAIMED IS:

1. A microarchitecture for an arithmetic unit, said arithmetic unit being defined to give a result on N bits ranked 0 to N-1 of an addition of at least two operands, and one corresponding output carry bit, said microarchitecture comprising a carry save adder to give two output vectors from at least two input operands, one of said operands corresponding to the current contents of an accumulator and a final adder receiving said vectors at input and giving a corresponding result at output wherein, in said microarchitecture, the carry save adder, the final adder and the accumulator are N+1 bit circuits, to apply the most significant N ranked bit of the result given by the said final adder and the most significant N ranked bit of the operand corresponding to the current contents of the accumulator to a circuit for determining said output carry bit.

2. A microarchitecture of an arithmetic unit according to claim 1, said carry save adder receiving a first operand, a second operand and a third operand as inputs, said third operand corresponding to the current contents of the accumulator, wherein said circuit for determining the output carry bit comprises a circuit for evaluating the most significant bit of the sum of said first and second input operands, or equivalent operands.

3. A microarchitecture according to claim 2, wherein said evaluation circuit comprises the necessary elements of an adder to give the most significant bit of said sum.

4. A microarchitecture according to claim 2 or 3, wherein the evaluated bit given by said evaluation

circuit, the N-ranked bit of the current contents of the accumulator and the N-ranked bit of the result given by the final adder are applied to an Exclusive-Or type logic circuit that outputs said output carry value.

5. A microarchitecture according to any one of claims 2 to 5 comprising a multiplier to give the partial products of two operands applied as inputs to the arithmetic unit, wherein said partial products are applied as first and second input operands of the carry save adder.

6. A microarchitecture according to claim 2, comprising a circuit for the concatenation of operands applied to the input of the arithmetic unit, giving a concatenated number at output, to carry out operations of double precision accumulation with the current contents of the accumulator, said concatenated number being applied as a first input operand of said carry save adder, said second operand being set at the zero vector.

7. A microarchitecture according to claim 6 taken in combination with claim 5, wherein the multiplier and the concatenation device are placed in parallel, a multiplexer circuit being designed to apply either the concatenated number and the zero vector or the partial products as the first and second input operands of the carry save adder, depending on whether the operation in progress uses the concatenation circuit or the multiplier.

8 A microarchitecture according to claim 7, wherein the circuit for determining the output carry bit comprises a multiplexer circuit to give, as an evaluated bit, either the bit given by the evaluation

circuit or the most significant bit of the concatenated number, depending on whether the operation in progress uses the concatenation circuit or the multiplier.

9. A microarchitecture according to claim 2 or 3, taken in combination with any of the claims 4 to 8, a format extension circuit being designed for the extension, to N^{+1} bits of the operands applied as first and second input operands of the carry save adder, wherein the circuit for the evaluation of the circuit for determining the output carry value receives as inputs, operands corresponding to said first and second input operands before format extension.

10. Microprocessor or microcontroller comprising an arithmetic unit having a microarchitecture according to any of the claims 1 to 9.